FIG.1

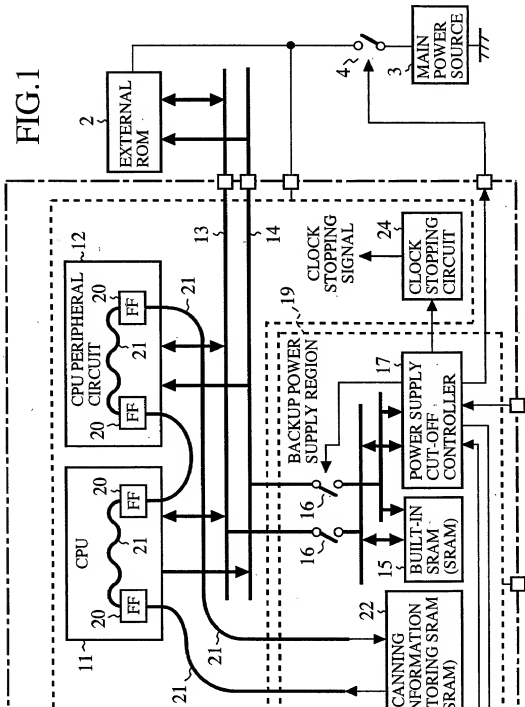
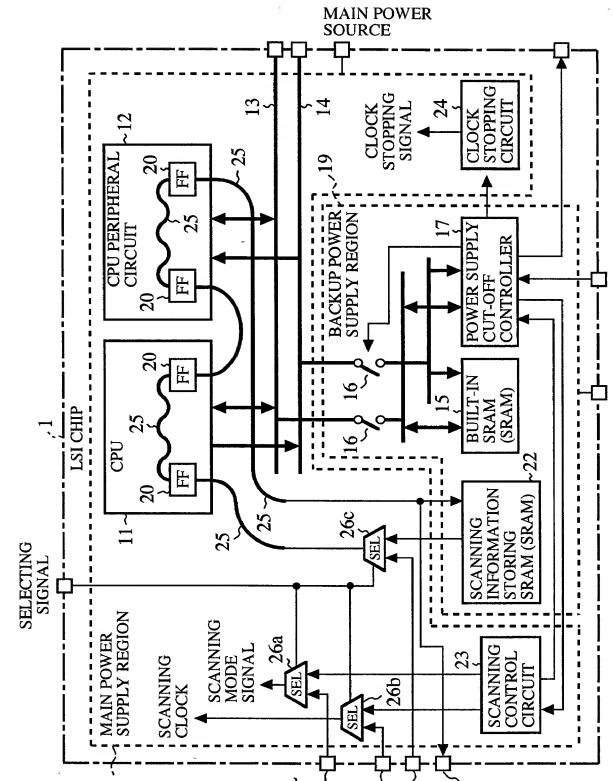

1
LSI CHIP
18
MAIN POWER SUPPLY REGION
SCANNING MODE SIGNAL
SCANNING CLOCK
23
SCANNING CONTROL CIRCUIT
11
CPU
20
FF
21
22
SCANNING INFORMATION STORING SRAM (SRAM)
12
CPU PERIPHERAL CIRCUIT
13
14
2
EXTERNAL ROM
4
3
MAIN POWER SOURCE
19
BACKUP POWER SUPPLY REGION
16
15
BUILT-IN SRAM (SRAM)
17
POWER SUPPLY CUT-OFF CONTROLLER
CLOCK STOPPING SIGNAL
24
CLOCK STOPPING CIRCUIT
6
RETURN TRIGGER CIRCUIT
5
BACKUP POWER SOURCE

FIG.2


MAIN POWER SOURCE
LSI CHIP
1
SELECTING SIGNAL
MAIN POWER SUPPLY REGION
18
SCANNING CLOCK
SCANNING MODE SIGNAL
26a
SEL
26b
SEL
26c
SEL
CPU
11
CPU PERIPHERAL CIRCUIT
12
FF
20
25
13
14
BACKUP POWER SUPPLY REGION
19
16
15
BUILT-IN SRAM (SRAM)
22
POWER SUPPLY CUT-OFF CONTROLLER
17
CLOCK STOPPING SIGNAL
24
CLOCK STOPPING CIRCUIT
SCANNING INFORMATION STORING SRAM (SRAM)
SCANNING CONTROL CIRCUIT
23
TEST MODE SIGNAL FOR SCAN TESTING
SCANNING CLOCK FOR SCAN TESTING
SCANNING INPUT SIGNAL FOR SCAN TESTING
SCANNING OUTPUT SIGNAL FOR SCAN TESTING

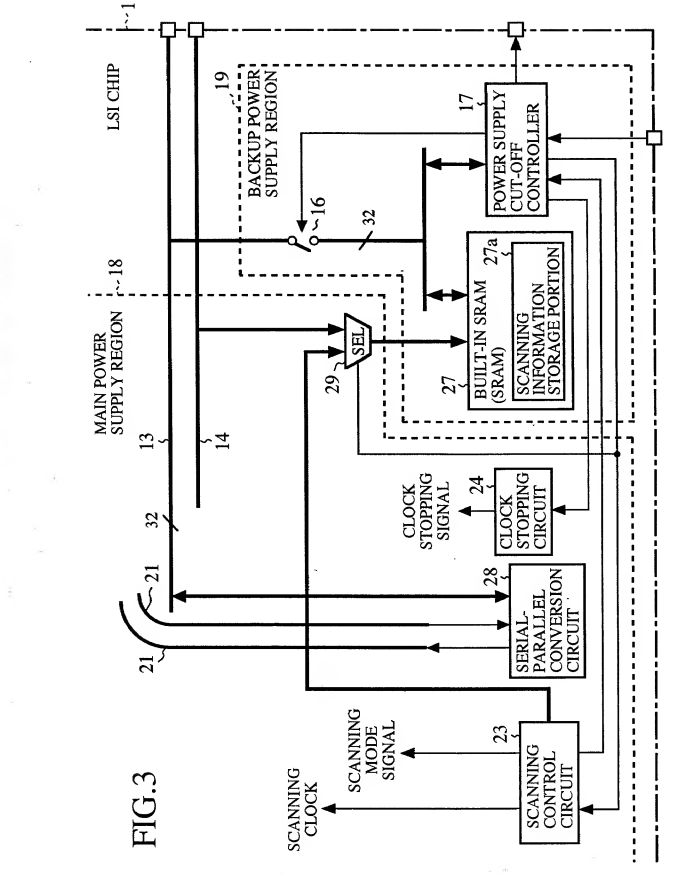

LSI CHIP
1
BACKUP POWER SUPPLY REGION
19
MAIN POWER SUPPLY REGION
18
POWER SUPPLY CUT-OFF CONTROLLER
17
16
32
27a
BUILT-IN SRAM (SRAM)
SCANNING INFORMATION STORAGE PORTION
27
SEL
29
13
14
CLOCK STOPPING SIGNAL
24
CLOCK STOPPING CIRCUIT
21
32
28
SERIAL-PARALLEL CONVERSION CIRCUIT
21
SCANNING MODE SIGNAL
23
SCANNING CLOCK
SCANNING CONTROL CIRCUIT

FIG.3

FIG.4

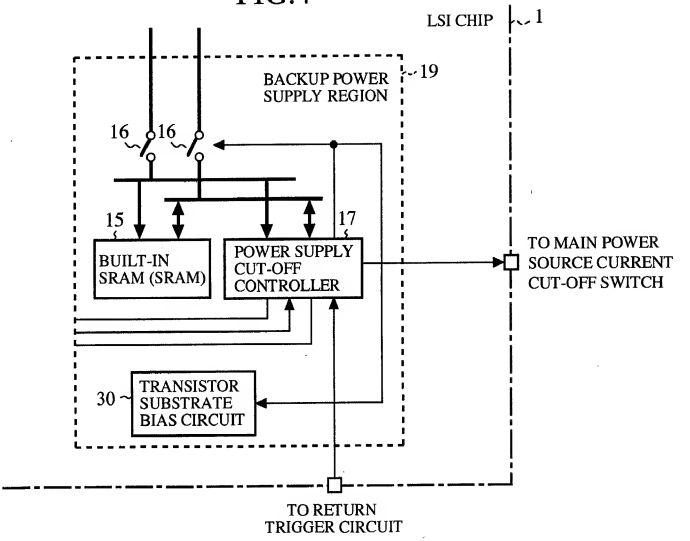

LSI CHIP
1
BACKUP POWER SUPPLY REGION
19
16
16
15
17
BUILT-IN SRAM (SRAM)
POWER SUPPLY CUT-OFF CONTROLLER
TO MAIN POWER SOURCE CURRENT CUT-OFF SWITCH
30
TRANSISTOR SUBSTRATE BIAS CIRCUIT
TO RETURN TRIGGER CIRCUIT

FIG.5

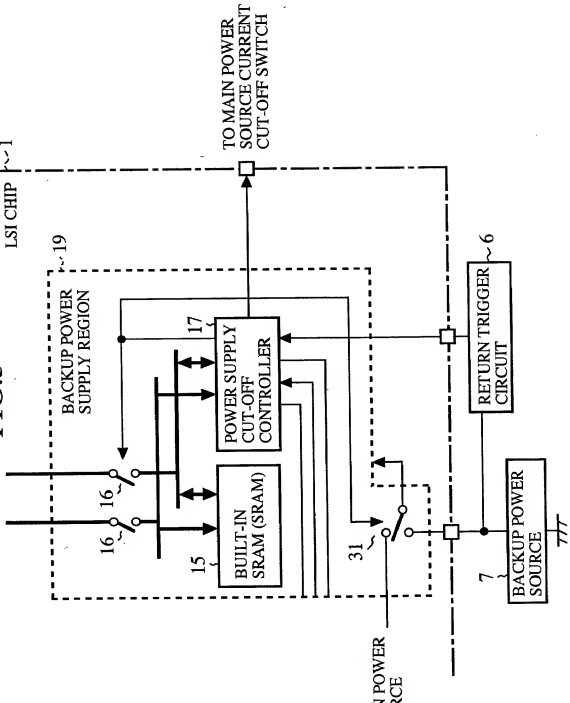
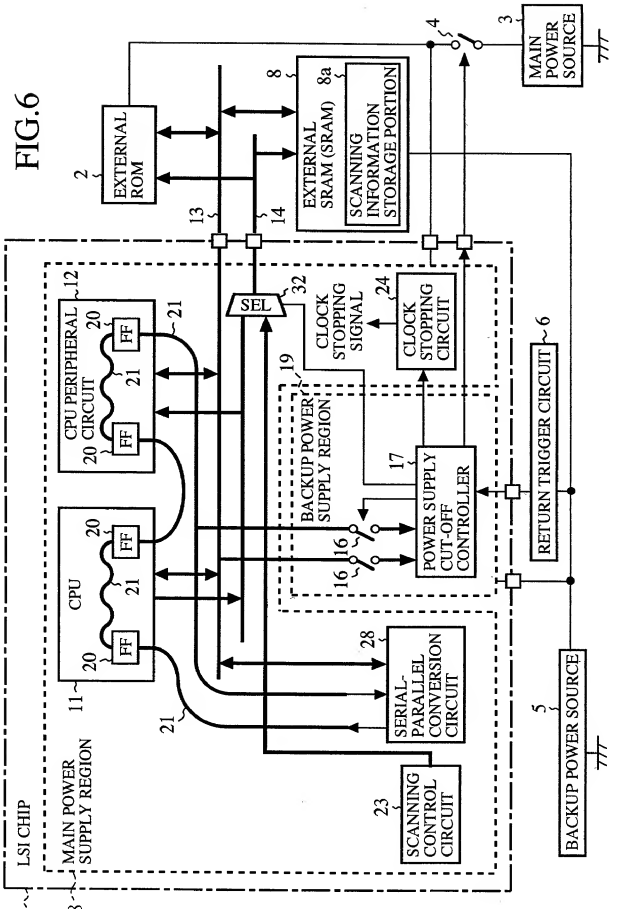

LSI CHIP
1
BACKUP POWER SUPPLY REGION
19
TO MAIN POWER SOURCE CURRENT CUT-OFF SWITCH
16
16
15
BUILT-IN SRAM (SRAM)
17
POWER SUPPLY CUT-OFF CONTROLLER
31
MAIN POWER SOURCE
RETURN TRIGGER CIRCUIT
6
7
BACKUP POWER SOURCE

FIG.6


LSI CHIP
MAIN POWER SUPPLY REGION
BACKUP POWER SUPPLY REGION
CPU
CPU PERIPHERAL CIRCUIT
FF
SEL
CLOCK STOPPING SIGNAL
CLOCK STOPPING CIRCUIT
POWER SUPPLY CUT-OFF CONTROLLER
SERIAL-PARALLEL CONVERSION CIRCUIT
SCANNING CONTROL CIRCUIT
RETURN TRIGGER CIRCUIT
BACKUP POWER SOURCE
MAIN POWER SOURCE
EXTERNAL ROM
EXTERNAL SRAM (SRAM)
SCANNING INFORMATION STORAGE PORTION

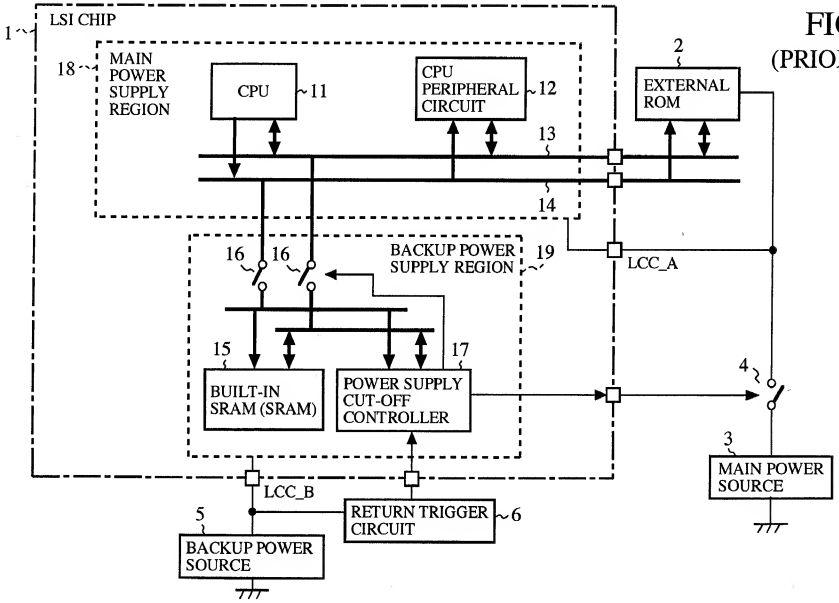


FIG.7
(PRIOR ART)